II Semester

Course 4: Digital Logic Design

Credits -3

Course Objectives

To familiarize with the concepts of designing digital circuits.

Course Outcomes

Upon successful completion of the course, the students will be able to

1. Understand how to Convert numbers from one radix to another radix and performarithmetic operations.
2. Simplify Boolean functions using Boolean algebra and k- maps
3. Design adders and subtractors circuits
4. Design combinational logic circuits such as decoders, encoders, multiplexers and demultiplexers.
5. Use flip flops to design registers and counters.

UNIT – I

Number Systems: Binary, octal, decimal, hexadecimal number systems, conversion of numbers from one radix to another radix, r's, (r-1)'s complements, signed binary numbers, addition and subtraction of unsigned and signed numbers, weighted and unweighted codes.

UNIT – II

Logic Gates and Boolean Algebra: NOT, AND, OR, universal gates, X-OR and X-NOR gates, Boolean laws and theorems, complement and dual of a logic function, canonical and standard forms, two level realization of logic functions using universal gates, minimizations of logic functions (POS and SOP) using Boolean theorems, K-map (up to four variables), don't care conditions.

UNIT – III

Combinational Logic Circuits – 1: Design of half adder, full adder, half subtractor, fullsubtractor, ripple adders and subtractors, ripple adder / subtractor.

UNIT – IV

Combinational Logic Circuits – 2: Design of decoders, encoders, priority encoder, multiplexers, demultiplexers, higher order decoders, demultiplexers and multiplexers, realization of Boolean functions using decoders, multiplexers.

UNIT – V

Sequential Logic Circuits: Classification of sequential circuits, latch and flip-flop, RS- latch using NAND and NOR Gates, truth tables, RS, JK, T and D flip-flops, truth and excitation tables, conversion of flip- flops, flip-flops with asynchronous inputs (preset and clear).

Text Books:

1. M. Morris Mano, Michael D Ciletti, “Digital Design”, 5th edition, PEA.

Reference Books

1. Kohavi, Jha, “Switching and Finite Automata Theory”, 3rd edition, Cambridge.
2. 2. Leach, Malvino, Saha, “Digital Principles and Applications”, 7th edition, TMH.
3. 3. Roth, “Fundamentals of Logic Design”, 5th edition, Cengage.

SUGGESTED CO-CURRICULAR ACTIVITIES & EVALUATION METHODS:

Unit 1: Activity: JAM (Just a Minute) Session: Explaining Radix Conversion
Evaluation Method: Communication Skills and Knowledge Presentation

Unit 2: Activity: Boolean Algebra Assignment
Evaluation Method: Assignment Completion and Correctness

Unit 3: Activity: Hands-on Lab Activity: Building Adder and Subtractor Circuits
Evaluation Method: Lab Performance and Correctness of Circuit Implementation

Unit 4: Activity: Group Discussion: Applications of Decoders, Encoders, Multiplexers
Evaluation Method: Participation and Critical Thinking

Unit 5: Activity: Quiz on Flip-Flops and Register-Counter Design
Evaluation Method: Quiz Performance and Knowledge Retention

II Semester

Course 4: Digital Logic Design

Credits -1

List of Experiments

The laboratory work can be done by using physical gates and necessary equipment or simulators.

Simulators: https://sourceforge.net/projects/gatesim/ or https://circuitverse.org/ or any free open-source simulator

1. Introduction to digital electronics lab- nomenclature of digital ICs, specifications, study of the data sheet, concept of Vcc and ground, verification of the truth tables of logic gates using TTL ICs.
2. Implementation of the given Boolean functions using logic gates in both SOP and POS forms
3. Realization of basic gates using universal gates.
4. Design and implementation of half and full adder circuits using logic gates.
5. Design and implementation of half and full subtractor circuits using logic gates.
6. Verification of stable tables of RS, JK, T and D flip-flops using NAND gates.
7. Verification of stable tables of RS, JK, T and D flip-flops using NOR gates.
8. Implementation and verification of Decoder and encoder using logic gates.
9. Implementation of 4X1 MUX and DeMUX using logic gates.
10. Implementation of 8X1 MUX using suitable lower order MUX.
11. Implementation of 7-segment decoder circuit.
12. Implementation of 4-bit parallel adder.
13. Design and verification of 4-bit synchronous counter.
14. Design and verification of 4-bit asynchronous counter.